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09/982,335	10/18/2001	Nobuaki Tsuji	PW 027 7019 H7601US	6722

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/982,335	Applicant(s) TSUJI ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,9,10,12,14-19 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,12,14-19 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a device comprising all the claimed limitations as recited in claim 5, wherein the semiconductor substrate serves as a base, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2.The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 23-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of high voltage of second and first polarity, corresponding to second and first conductivity types, respectively, as

recited in claims 23-26, are unclear as to how a voltage can be correlated to a conductivity type.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5 and 23-26, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (6,281,527) in view of Applicant Admitted Prior Art (AAPA).

Chen teaches in figure 3 and related text an input protection circuit comprising: a semiconductor substrate 30 of a first conductivity type; a first well region 31 of a second conductivity type opposite to the first conductivity type, the first well region being formed in one principal surface area of the semiconductor substrate and forming a PN junction with the semiconductor substrate; first and second impurity doped regions 33, 32 of the first conductivity type formed in the first well region and forming a first lateral bipolar transistor with a portion of the first well region serving as a base; a second well region 40 of the first conductivity type formed in the principal surface area of the

semiconductor substrate; third and fourth regions 36, 34 of the second conductivity type formed in the second well region and forming a second lateral bipolar transistor with a portion of the second well region serving as a base, bottoms of the third and fourth well regions forming a PN junction with the second well or with the semiconductor substrate, an input terminal 1 formed on the semiconductor substrate; a circuit formed in the semiconductor substrate, and connected to the input terminal; and a reference potential node Vss formed on the semiconductor substrate; wherein the first and second lateral bipolar transistors are connected in series between the input terminal and the reference potential node, wherein the input terminal is connected to the first impurity doped region, the second impurity doped region and the base of the first lateral bipolar transistor are connected to the third well region, the first lateral bipolar transistor operating without a fixed base bias, and the fourth well region and the base of the second lateral bipolar transistor are connected to the reference potential node.

Chen does not teach third and fourth regions being third and fourth well regions.

AAPA teaches in figure 10 third and fourth regions 5, 6 being formed in third and fourth well regions 3, 4.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth regions in third and fourth well regions

in Chen's device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claim 5, a portion of the semiconductor substrate serves as a base in Chen's device, because the P type substrate and the P well base region have the same conductivity type, thus rendering the substrate as being part of the base region.

Regarding claims 23-26, the claimed limitations of first and second lateral bipolar transistors being turned on to protect the input protection circuit when a high voltage of second and first polarity, corresponding to second and first conductivity types, respectively, are applied to the input terminal, are inherent in Chen's device, because Chen's structure is identical to the claimed structure.

6. Claims 5 and 25-26, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Groeseneken et al. (6,570,226) in view of Applicant Admitted Prior Art (AAPA).

Groeseneken et al. teach in figure 5 and related text an input protection circuit comprising: a semiconductor substrate of a first conductivity type; a first well region 51 of a second conductivity type opposite to the first conductivity type, the first well region being formed in one principal surface area of the semiconductor substrate and forming

a PN junction with the semiconductor substrate; first and second impurity doped regions 541, 542 of the first conductivity type formed in the first well region and forming a first lateral bipolar transistor with a portion of the first well region serving as a base; third and fourth regions 551, 552 of the second conductivity type formed in the semiconductor substrate and forming a second lateral bipolar transistor with a portion of the semiconductor substrate serving as a base; a circuit formed in the semiconductor substrate, and connected to the input terminal; and a reference potential node Vss formed on the semiconductor substrate; wherein the first and second lateral bipolar transistors are connected in series between the input terminal and the reference potential node, wherein the input terminal is connected to the first impurity doped region, the second impurity doped region and the base of the first lateral bipolar transistor are connected to the third well region, the first lateral bipolar transistor operating without a fixed base bias, and the fourth well region and the base of the second lateral bipolar transistor are connected to the reference potential node.

Note that the broad recitation of the claim does not require the base of the first lateral bipolar transistor to be directly connected to the third well region.

Groeseneken et al. do not teach third and fourth regions being third and fourth well regions.

AAPA teaches in figure 10 third and fourth regions 5, 6 being formed in third and fourth well regions 3, 4.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth regions in third and fourth well regions in Groeseneken et al.'s device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claims 25-26, the claimed limitations of first and second lateral bipolar transistors being turned on to protect the input protection circuit when a high voltage of second and first polarity, corresponding to second and first conductivity types, respectively, are applied to the input terminal, are inherent in Groeseneken et al.'s device, because Groeseneken et al.'s structure is identical to the claimed structure.

7. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and AAPA, as applied to claims 1 and 5 above, and further in view of Watt (5,477,413).

Regarding claims 2 and 6, Chen and AAPA teach substantially the entire claimed structure, as applied to claims 1 and 5 above, including a current limiting resistor R1 (Chen, figure 4) formed on a principal surface area of the semiconductor substrate, wherein the input terminal is connected via the current limiting resistor to the first impurity doped region, and an insulating layer 8 (AAPA, figure 10) formed in the

principal surface area of the semiconductor substrate. Chen and AAPA do not explicitly state forming the resistor on the semiconductor substrate.
Watt teaches in figure 5 forming resistor 58 on the semiconductor substrate (column 7, lines 29-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the resistor on the semiconductor substrate in Chen and AAPA's device, in order to provide better control over the resistance value and thus the characteristics of the device.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Groeseneken et al. and AAPA, as applied to claim 5 above, and further in view of Watt (5,477,413).
Regarding claim 6, Groeseneken et al. and AAPA teach substantially the entire claimed structure, as applied to claim 5 above, including a current limiting resistor R1 (Groeseneken et al., figure 6) formed on a principal surface area of the semiconductor substrate, wherein the input terminal is connected via the current limiting resistor to the first impurity doped region, and an insulating layer 8 (AAPA, figure 10) formed in the principal surface area of the semiconductor substrate. Groeseneken et al. and AAPA do not explicitly state forming the resistor on the semiconductor substrate.
Watt teaches in figure 5 forming resistor 58 on the semiconductor substrate (column 7, lines 29-35). It would have been obvious to a person of ordinary skill in the art at the

time the invention was made to form the resistor on the semiconductor substrate in Groeseneken et al. and AAPA's device, in order to provide better control over the resistance value and thus the characteristics of the device.

9. Claims 9 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (3,955,210).

Bhatia et al. teach in figure 3 and related text a semiconductor input protection circuit comprising: a semiconductor substrate 2; a first active region 4 of a first conductivity type defined in the semiconductor substrate; a second active region 6 of a second conductivity type defined in the semiconductor substrate; first and second impurity doped regions 22, 20 of the second conductivity type formed in the first active region; third and fourth impurity doped regions 15, 18 of the first conductivity type formed in the second active region; a terminal +VH connected to the first impurity doped region 22; a first wiring for connecting the first active region and the second impurity doped region 20 to the third impurity doped region 15; and a second wiring for connecting the second active region and the fourth impurity doped region 18 to a reference potential +VH.

Bhatia et al. do not state that terminal +VH is an input terminal.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use terminal +VH as an input terminal in Bhatia et al.'s device, in order to operate the device in its intended use.

Regarding claim 15, Bhatia et al. teach in figure 3 a first contact region 23 of the first conductivity type having a high impurity concentration, and formed in the first active region outside the first and second impurity doped regions, wherein the first wiring is connected via the first contact region 23 to the first active region 4.

Regarding claim 17, Bhatia et al. teach in figure 3 a second contact region 14 of the second conductivity type having a high impurity concentration, and formed in the second active region outside the third and fourth impurity doped regions, wherein the second wiring is connected via the second contact region 14 to the second active region 6.

Regarding claims 16 and 18, Bhatia et al. teach in figure 3 a first contact region and the third and fourth impurity doped regions and a second contact region and the first and second impurity doped regions have substantially the same impurity concentration and depth, respectively.

10. Claims 10, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. (5,747,837) in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 10, Bhatia et al. teach substantially the entire claimed structure, as applied to claim 9 above, except third and fourth impurity doped well regions reaching a

bottom of the second active region. AAPA teaches in figure 10 the third and fourth impurity doped well regions 3, 4 reach a bottom of the second active region.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the third and fourth regions to reach a bottom of the second active region in Bhatia et al.'s device, in order to provide high inverse breakdown voltage to the protection device.

Regarding claim 19, Bhatia et al. and AAPA teach a first contact region 23 (Bhatia et al., figure 3) of the first conductivity type having a high impurity concentration, and formed in the first active region outside the first and second impurity doped regions, wherein the third and fourth impurity doped regions each include a surface side high impurity concentration region and a deeper low impurity concentration region, and have substantially the same impurity concentration and depth as the surface side high impurity concentration region and the first contact region.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatia et al. in view of Iwase et al. and Watt.
Bhatia et al. teach substantially the entire claimed structure, as applied to claim 9 above, including an insulating film 62 (figure 5) formed on the semiconductor substrate. Bhatia et al. do not teach forming a polysilicon resistor on the insulating film, wherein

the input terminal is connected via the polysilicon resistor to the first impurity doped region.

Iwase et al. teach in figure 1 an input terminal is connected via a resistor to the first impurity doped region. Watt teaches in figure 5 forming polysilicon resistor 58 on the semiconductor substrate (column 7, lines 29-35). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to a polysilicon resistor on the insulating film, wherein the input terminal is connected via the polysilicon resistor to the first impurity doped region in Bhatia et al.'s device, in order to provide better control over the resistance value and thus improve the characteristics of the device.

Response to Arguments

12. Applicant argues that it would not be obvious to replace the input with the voltage potential terminal in Bhatia's device.

It would have been obvious to an artisan to use terminal +VH as an input terminal in Bhatia et al.'s device, in order to operate the device in its intended use. Note that the device does not serve any purpose without an input terminal.

13. Applicant's arguments with respect to claims 1-2, 5-6 and 23-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG

30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
June 25, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800